TrellisWare F-LDPC FEC

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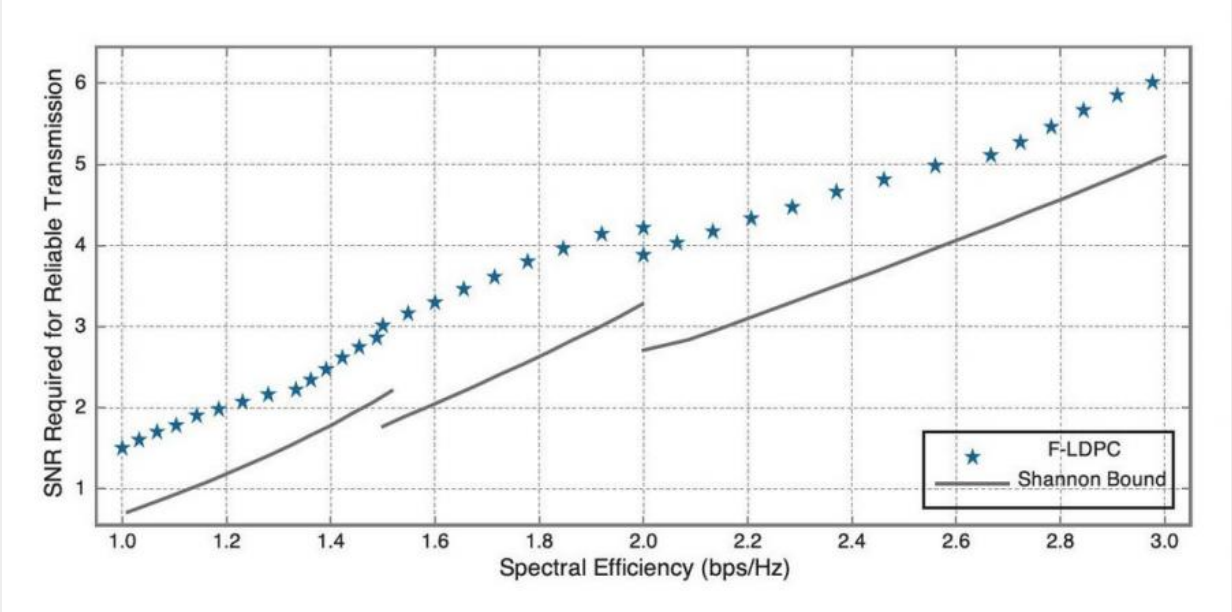
TrellisWare Flexible-Low Density Parity Check (F-LDPC)

TrellisWare designed the F-LDPC code family to meet the demand for high-performance Forward Error Correction (FEC) solutions across a wide range of commercial and military applications. F-LDPC codes offer capacity-approaching performance for all offered code rates and modulations without sacrificing decoder latency or throughput.

F-LDPC is available as encoder and decoder cores for FPGA and ASIC devices. Standard cores support 8 block sizes, 40 code rates, 4 modulation types and can be instantaneously reconfigured on-the-fly: there is zero latency penalty when transitioning from decoding a 128-bit, rate-1/2, QPSK-modulated data block to a 16,384-bit, rate-32/33, 16QAM-modulated data block.
TrellisWare can also add custom block sizes and code rates before or after delivery via a simple, programmable ROM update.

F-LDPC is deployed in very small aperture terminals (VSAT), free space optics (FSO), holographic storage systems, military waveforms, and TrellisWare's own tactical mobile ad-hoc networking (MANET) radio products. Some customers choose the F-LDPC for its throughput – Gpbs+ in FPGAs – while others value its low implementation complexity. Others leverage the flexibility of the F-LDPC while designing new waveforms, or for backwards compatibility with legacy links.

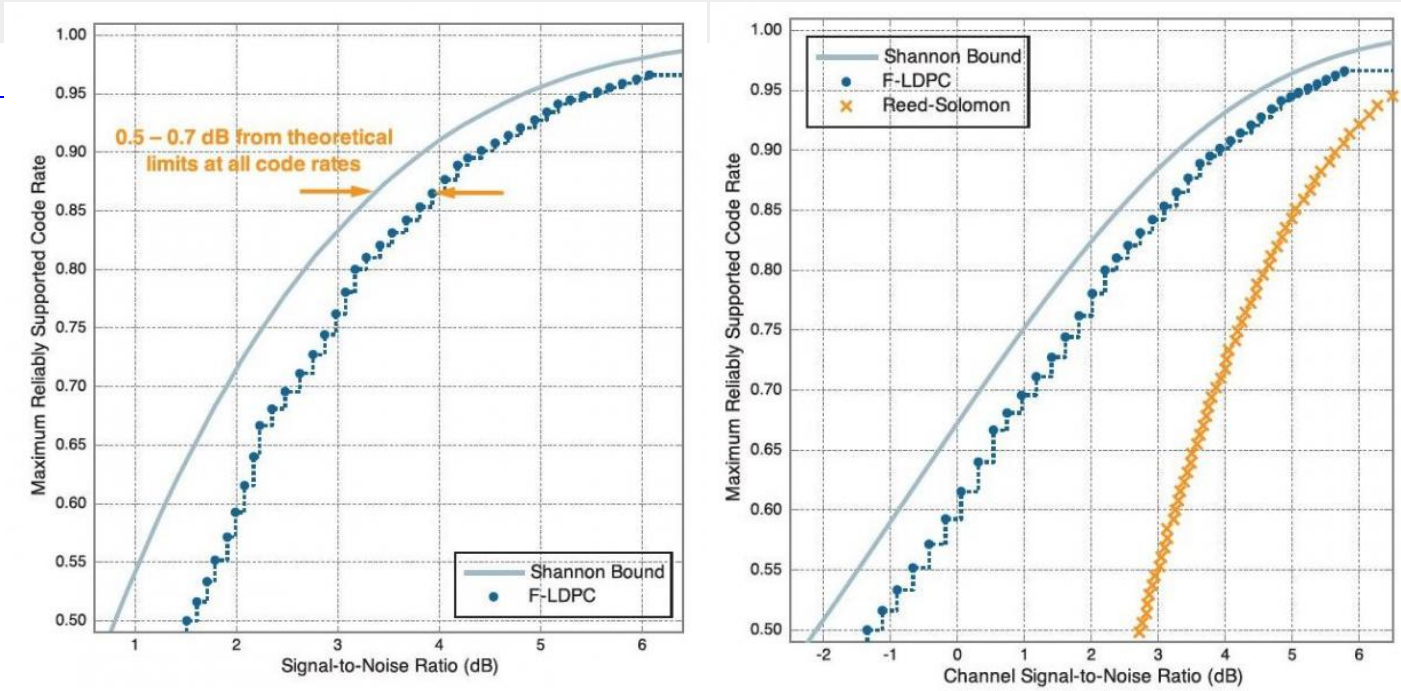


The F-LDPC provides performace within 1 dB of information-theoretic bounds across all code rates and modulations. This is achieved with a low-complexity, high-throughput decoding architecture.

The flexible, capacity-approaching threshold performance, and excellent floor performance of F-LDPC make it appealing to customers across diverse markets, with diverse applications:

- ☑ Replace Viterbi/Reed Solomon FEC with a modern code without changing other elements of waveform design
- ☑ Apply it to low-cost VSAT and M2M communications links
- ☑ E Band and optical link designers use it to benefit from modern codes at multi-Gbps throughputs

AT



Features

UNPARALLELED FLEXIBILITY

- ☑ Single encoder/decoder core supports 40 code rates (1/2–32/33) and multiple block sizes. Default block sizes are 128, 256, 512, …, 16384 bits
- ☑ Single encoder/decoder core supports any block size, code rate, and modulation combination
- ☑ Configurable on the fly: Block to block changes with zero latency
- ☑ Custom block sizes and code rates can be added to standard cores

PROVEN PERFORMANCE

- ☑ Capacity approaching performance with low implementation complexity; maximizes Message Completion Rate (MCR)
- ☑ Low error floors
- ☑ High performance for small block sizes

HIGH-THROUGHPUT, LOW-COMPLEXITY

- ✅ Up to 10 Gbps throughput in a single FPGA
- ✅ 100 Gbps+ throughputs achievable in ASICs
- ✅ Complexity lower than competing LDPC and turbo codes

TrellisWare - F-LDPC FEC - Modern Forward Error Correction